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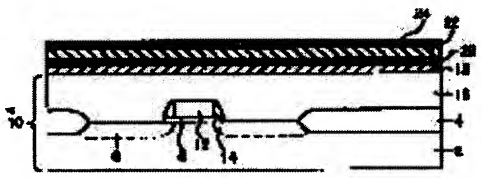
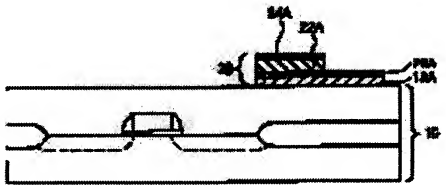
(54) SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

(57)Abstract:

PROBLEM TO BE SOLVED: To prevent the occurrence of leakage current which is caused in pzt by forming a transistor on a semiconductor substrate, forming an active substrate containing an insulating layer on the transistor and an isolation region, thereafter forming a lower electrode on the insulating layer, positioning a capacitor thin film on the lower electrode, and forming an upper electrode on the thin film.



SOLUTION: A MOS transistor as an selective transistor and an isolation region 4 are formed on a silicon substrate 2, and a first insulating layer 16 is formed on the MOS transistor and the isolation region 4 to form an active substrate 10. A lower electrode 20A is formed on the first insulating layer 16 of the active substrate 10, and the first insulating layer 16 and the lower electrode 20A are bonded together with a buffer 18A in-between. Further, a capacitor thin film 22A is formed on the lower electrode 20A, and an upper electrode 24A is formed on the capacitor thin film 22A to form a capacitor structure 23.



LEGAL STATUS

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CLAIMS

[Claim(s)]

[Claim 1] The transistor formed on a semi-conductor substrate and the above-mentioned semi-conductor substrate in the semiconductor device used for a memory cell, The active substrate containing the insulating layer formed on the isolation field for carrying out the isolation (isolation) of the above-mentioned transistor, the above-mentioned transistor, and the above-mentioned isolation field, It is formed on the above-mentioned insulating layer, and is located on a lower electrode and the above-mentioned lower electrode. The semiconductor device characterized by including the capacitor structure which consists of an up electrode formed on the capacitor thin film which consists of PZT (lead zirconate titanate) (PNZT) by which Nb was doped, and the above-mentioned capacitor thin film.

[Claim 2] The above-mentioned semi-conductor substrate is a semiconductor device according to claim 1 characterized by consisting of silicon (Si).

[Claim 3] The above-mentioned insulating layer is a semiconductor device according to claim 2 characterized by consisting of oxide like silicon oxide (SiO2).

[Claim 4] The above-mentioned lower electrode is a semiconductor device according to claim 3 characterized by consisting of platinum (Pt) / titanium (Ti).

[Claim 5] The above-mentioned capacitor thin film is a semiconductor device according to claim 1 characterized by being formed using Pb and an alkoxide (alkoxide).

[Claim 6] Above PNZT is a semiconductor device according to claim 1 with which it forms using the sol gel coating solution (sol-gel coating solution) shown by formula Pb(1-x/2) Pbx(Zr0.52Ti0.48) (1-x) O3, and Nb is characterized by compensating the charge generated by the vacancy (vacancy) of Pb (compensate) when x is 0-0.05.

[Claim 7] The step which prepares the active substrate equipped with the insulating layer formed around a transistor and the above-mentioned transistor in the semiconductor device manufacture approach used for a memory cell, b) The step which is formed on the above-mentioned insulating layer and forms the capacitor structure containing the capacitor thin film which consists of PNZT, c) -- in order to form the 1st metal layer and to connect the above-mentioned transistor to the above-mentioned capacitor structure electrically -- the 1st metal layer -- the 1st -- the semiconductor device manufacture approach characterized by including the step which carries out pattern NINGU in the already set-up configuration.

[Claim 8] The step at which the above-mentioned b step forms the 1st metal layer on the b1 above-mentioned insulating layer, The step which forms the above-mentioned capacitor thin film on the 1st

metal layer of b2 above, The step which forms the 2nd metal layer on the b3 above-mentioned capacitor thin film layer, the 2nd metal layer of b4 above, and the above-mentioned capacitor thin film -- the 1st -- the configuration set up beforehand -- pattern NINGU -- carrying out -- the above-mentioned 1st metal layer -- the 2nd -- the semiconductor device manufacture approach according to claim 7 characterized by including the step which carries out pattern NINGU at the configuration set up beforehand, and obtains the above-mentioned capacitor structure.

[Claim 9] It is the semiconductor device manufacture approach according to claim 8 characterized by annealing and (anneal) making the above-mentioned capacitor thin film into the temperature which has the range from about 500 degrees C to about 700 degrees C with oxygen gas after the above-mentioned step b4.

[Claim 10] The above-mentioned annealing process is the semiconductor device manufacture approach according to claim 9 characterized by being carried out for about 30 minutes.

[Claim 11] The above-mentioned semi-conductor substrate is the semiconductor device manufacture approach according to claim 10 characterized by consisting of Si.

[Claim 12] The above-mentioned insulating layer is SiO2. The semiconductor device manufacture approach according to claim 11 characterized by consisting of oxide [like].

[Claim 13] The above-mentioned 1st metal layer is the semiconductor device manufacture approach according to claim 12 characterized by consisting of Pt/Ti.

[Claim 14] Above PNZT is the semiconductor device manufacture approach according to claim 7 that it forms using the sol gel coating solution shown by formula Pb(1-x/2) Pbx(Zr0.52Ti0.48) (1-x) O3, and Nb is characterized by compensating the charge generated by the vacancy of Pb when x is 0-0.05.

[Claim 15] The step which the b2 above-mentioned step prepares b21 pulley cursor (precursors) P1, P2, and P3 and P4, b22P1 The step in which P1 which carried out the dehydration-ized reaction (dehydrating) and dehydration--ization-reacted to 2-methoxyethanol (2-methoxyethanol) is dissolved (dissolve), P(dissolved) 1 by which the b23 above-mentioned dissolution was carried out In the step which is mixed under vacuum (mixing) and obtains a Pb-Nb solution, and b24 inert-gas ambient atmosphere Above P3 And the step which mixes the above P4 and obtains a Zr-Pb solution, The step which makes a b25 above-mentioned Pb-Nb solution and the above-mentioned Zr-Pb solution flow back (reflux), The step which adds NH4OH for b26 basic acceleration conditions (base-catalyzed condition), The step which adds ethylene glycol (ethylene glycol) by kind of b27 desiccation control chemistry additive (dry control chemical additive), and obtains a sol gel coating solution, The semiconductor device manufacture approach according to claim 10 characterized by including the step which carries out spin coating of the above-mentioned sol gel coating solution, and forms the above-mentioned capacitor thin film on the 1st metal layer of b28 above.

[Claim 16] The semiconductor device manufacture approach according to claim 8 characterized by including further the step for annealing the above-mentioned capacitor thin film at low temperature before the above-mentioned b3 step.

[Claim 17] In the approach of forming sol gel coating **, in order to make the ferroelectric matter a) The pulley cursor P1, P2, and P3 And the step which prepares P4, b) P1 The step in which P1 to which the dehydration-ized reaction (dehydrating) was carried out under vacuum, and the vacuum dehydration--ization-reacted to 2-methoxyethanol (2-methoxyethanol) is dissolved, c) P(dissolved) 1 by which the dissolution was carried out [above-mentioned] And P2 The step which is mixed under vacuum (mixing)

and obtains a Pb-Nb solution, d) It is the above P3 in an inert gas ambient atmosphere. And the above P4 The step which is mixed and obtains a Zr-Pb solution, e) The step which makes the above-mentioned Pb-Nb solution and the above-mentioned Zr-Pb solution flow back, f) The step which adds NH4OH for basic acceleration conditions (base-catalyzed condition), g) Ethylene glycol (ethylene glycol) is added by kind of a desiccation control chemistry additive (dry control chemical additive). The semiconductor device manufacture approach characterized by including the step which obtains a sol gel coating solution.

[Claim 18] Above P1 For Nb-PENTA ethoxide (penta ethoxide) and P3, Pb-acetate tree hydrate (acetatetrihydrate) and P2 are [Zr-Normal propoxide (normal propoxide) and P4] the semiconductor device manufacture approach according to claim 17 characterized by being Ti-isopropoxide (iso propoxide).

[Claim 19] The above-mentioned b step is the semiconductor device manufacture approach according to claim 18 characterized by performing by the excess (excess) Pb of about 5 mall (mole) %.

[Claim 20] The above-mentioned Zr-Pb solution is the semiconductor device manufacture approach according to claim 19 characterized by preparing on air conditions.

[Claim 21] The above-mentioned e step is the semiconductor device manufacture approach according to claim 20 characterized by performing 1 hour at about 106 degrees C.

[Claim 22] The above-mentioned d step is the above P3. And the semiconductor device manufacture approach according to claim 21 characterized by including further the step for diluting the above P4 (diluting).

[Claim 23] The semiconductor device manufacture approach according to claim 22 characterized by including further the step for carrying out keel rating (chealating) of the P3 and P4 by which dilution was carried out [above-mentioned] after the above-mentioned dilution step.

[Claim 24] d) P3 by which dilution was carried out [above-mentioned] after the step And the semiconductor device manufacture approach according to claim 21 characterized by including further the step for carrying out keel rating of P4.

[Claim 25] c) A step is the semiconductor device manufacture approach according to claim 17 characterized by performing by inert gas.

[Claim 26] The above-mentioned sol gel coating solution is the semiconductor device manufacture approach according to claim 17 that it is shown by formula Pb(1-x/2) Pbx(Zr0.52Ti0.48) (1-x) O3, and Nb is characterized by compensating the charge generated by the vacancy of Pb when x is 0-0.05.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[The technical field to which invention belongs] Especially this invention relates to the semiconductor device which has the ferroelectric capacitor structure used for a memory cell, and its manufacture approach about a semiconductor device.

[0002]

[Description of the Prior Art] DRAM (dynamic random access memory) which has the memory cell constituted by the transistor and the capacitor will have a still higher degree of integration general and by mainly being miniaturized through detailed-izing (micronization). However, there is a demand which still miniaturizes memory cell area.

[0003] In order to reduce the cel area which can be used for a capacitor in response to such a demand, various approaches like the trench mold arranged by the memory device in three dimensions or a stack mold have been proposed. However, the production process of the capacitor arranged in three dimensions is long, and it it is not only tedious, but is accompanied by the high production cost as a result. Therefore, a complicated manufacture step is not required, but there is a strong demand to the new memory device which can reduce cel area, securing the information on an initial complement.

[0004] As an attempt for making the above-mentioned demand satisfy, the ferroelectric random-access memory (FeRAM) for which the capacitor thin film which has strong dielectric characteristics is used as a capacitor thin film has been proposed like BST (barium strontium titanate).

[0005] However, typical PZT has some faults in using it for FeRAM. For the volatility of PbO, I hear that floating classes (mobile species) like a migration metal ion and Pb vacancy gather for one place intensively, and one of the main faults of PZT has them. Consequently, this phenomenon generates the leakage current (leakage current) which occurs in PZT.

[0006]

[Problem(s) to be Solved by the Invention] Therefore, this invention has the object in offering the semiconductor device which has a ferroelectric capacitor containing Nb doped by PNZT, and its manufacture approach.

[0007]

[Means for Solving the Problem] In the semiconductor device which uses this invention for a memory cell in order to attain the above-mentioned object The isolation field for carrying out the isolation (isolation) of the transistor and the above-mentioned transistor which are formed on a semi-conductor substrate and the above-mentioned semi-conductor substrate, And the active substrate containing the insulating layer formed on the above-mentioned transistor and the above-mentioned isolation field, It is formed on the above-mentioned insulating layer, and is located on a lower electrode and the above-mentioned lower electrode. The semiconductor device containing the capacitor structure which consists of an up electrode formed on the capacitor thin film which consists of PZT (lead zirconate titanate) (PNZT) by which Nb was doped, and the above-mentioned capacitor thin film is offered.

[0008] Moreover, this invention is set to the semiconductor device manufacture approach used for a memory cell. a) The step which prepares an active substrate equipped with the insulating layer formed around the transistor and the above-mentioned transistor, b) The step which is formed on the above-mentioned insulating layer and forms the capacitor structure containing the capacitor thin film which consists of PNZT, c) -- in order to form the 1st metal layer and to connect the above-mentioned transistor to the above-mentioned capacitor structure electrically -- the 1st metal layer -- the 1st -- the semiconductor device manufacture approach which contains the step which carries out pattern NINGU in the already set-up configuration is offered.

[0009] Moreover, this invention is set to the approach of forming a sol gel coating solution, in order to make the ferroelectric matter. a) The pulley cursor P1, P2, and P3 And the step which prepares P4, b) P1 The step in which P1 to which the dehydration-ized reaction (dehydrating) was carried out under

vacuum, and the vacuum dehydration--ization-reacted to 2-methoxyethanol (2-methoxyethanol) is dissolved, c) P(dissolved) 1 by which the dissolution was carried out [above-mentioned] And P2 The step which is mixed under vacuum (mixing) and obtains a Pb-Nb solution, d) It is the above P3 in an inert gas ambient atmosphere. And the above P4 The step which is mixed and obtains a Zr-Pb solution, e) The step which makes the above-mentioned Pb-Nb solution and the above-mentioned Zr-Pb solution flow back, f) The step which adds NH4OH for basic acceleration conditions (base-catalyzed condition), g) Ethylene glycol (ethylene glycol) is added by kind of a desiccation control chemistry additive (dry control chemical additive). The semiconductor device manufacture approach containing the step which obtains a sol gel coating solution is offered.

[0010]

[Embodiment of the Invention] In order to form the sectional view of the semiconductor device 100 used for a memory cell, the sectional view showing the manufacture approach, and a ferroelectric thin film, the flow chart which shows the process for which a solution is prepared is shown to drawing 1 , drawing 2 , or drawing 6 by the desirable example of this invention. In addition, the same sign is given to the same part shown in drawing 1 , drawing 2 , or drawing 6 .

[0011] In order to explain to a detail so that those who have hereafter the information usual by the technical field to which this invention belongs can carry out technical thought of this invention easily, it explains with reference to the drawing which attached the desirable example of this invention.

[0012] The sectional view of the semiconductor device 100 including the capacitor structure 23 formed on the active substrate 10 which contains an MOS transistor in drawing 1 , and the active substrate 10, the bit line 34, the metal interconnect 36, and the plate line 38 is shown. An active substrate 10 contains the insulating layer 16 formed on the isolation field 4 for carrying out the isolation of the semi-conductor substrate 2 and the MOS transistor, the MOS transistor, and the isolation field 4. An MOS transistor contains further the gate oxide 8, the gate line 12, and a spacer 14. In the desirable example, the semi-conductor substrate 2 consists of silicon (Si), and if an insulating layer 16 consists of a silicon oxide (SiO2), lower electrode 29A will consist of platinum (Pt). In order to raise adhesive strength among insulating-layer 16 and lower electrode 20A, buffer 18A which consists of titanium (Ti) can be used.

[0013] Although the capacitor structure 23 is located on lower electrode 20A, it contains capacitor thin film 22A which consists of PNZT, and up electrode 24A formed on capacitor thin film 22A. In this example, PNZT is formed using Pb and an alkoxide.

[0014] Although the bit line 34 is electrically connected to any one of the diffusion fields 6 and lower electrode 20A is electrically connected to other remaining diffusion fields 6 through the metal interconnect 36 with a semiconductor device 100, the bit line 34 and metal interconnect are made to separate mutually electrically in this case. In order to impress common constant potential, up electrode 24A is connected to the plate line 38.

[0015] The manufacture step relevant to the semi-conductor memory device manufacture approach which starts this invention at drawing 2 thru/or drawing 6 is shown.

[0016] The production process of a semiconductor device 100 starts preparing the active substrate 10 containing the 1st insulating layer 16 formed on a silicon substrate 2, the MOS transistor formed on it as an alternative transistor, the isolation field 4, the MOS transistor, and the isolation field 4. The 1st insulating layer 16 which consists of a silicon oxide (SiO2) over all front faces by plasma CVD (chemical vapor deposition) is formed. An MOS transistor includes the diffusion field 6, the gate oxide 8, the spacer

14, and the gate line 12 of the couple which acts as the source and a drain.

[0017] At the following step, as shown in drawing 2 , a buffer layer 18, the 1st metal layer 20, and a dielectric layer 22 are formed in order on an active substrate 10. A buffer layer 18 consists of titanium (Ti), and the 1st metal layer 20 consists of platinum (Pt). A buffer layer 18 and the 1st metal layer 20 are made to vapor-deposit using an approach like sputtering (sputtering). Although a dielectric layer 22 consists of ferroelectric matter, the manufacture approach is explained to a detail below with drawing 7 .

[0018] The 1st step 50 of a process is a step which prepares pulley cursor (precursors), such as P1, P2, and P3, P4. For P1, as for Nb-PENTA ethoxide (penta ethoxide) and P3, in the desirable example, Pb-acetate tree hydrate (acetate trihydrate) and P2 are [Zr-Normal propoxide (normal propoxide) and P4] Ti-isopropoxide (iso propoxide). At step 52, the dehydration-ized reaction (dehydrated) of the pulley cursor P1 is carried out under vacuum as excess Pb of 5 mall (mole) %. Subsequently, the pulley cursor P1 which dehydration--ization-reacted is dissolved in 2-methoxyethanol (2-methoxyethanol) at step 58. The dissolved pulley cursor P3 and P4 is mixed at step 62, and a Pb-Nb solution is obtained.

[0019] On the other hand, the pulley cursor P3 and P4 is made to dilute with each of steps 54 and 56 with a suitable solvent (solvent) like PrOH (propanol) (dilute). In order to lower the magnetic susceptibility (susceptibility) of the alkoxide to hydrolysis (hydrolysis) at the following step 60, keel rating (chealate) of the pulley cursor P3 and P4 is carried out to EacAc (ethylacetoacetate), and a Zr-Pb solution is prepared on the air conditions of step 64. It is possible to perform the keel rhe SHON (chealation) step 60 after step 64.

[0020] A Zr-Pb solution and a Pb-Nb solution are made to flow back at the temperature which has the range from about 60 degrees C to about 100 degrees C at step 66 (refluxing). At the following step, for basic acceleration conditions (base-crystalized condition), a catalyst (H2 O+NH4 OH+PrOH) like 0.05 mall (mol) NH4OH is added to step 68, and it changes to a PNZT stock solution (stock solution) at it. The PNZT solution with which the PNZT stock solution was made to add ethylene glycol (ethylene glycol) by DCCA (dry control chemical additive), and it stabilized for ferroelectric thin layer coating at step 70 after partial hydrolysis (hydrolysis) is obtained. Although the ferroelectric thin film doped by 0.3MNb (doped) is prepared in the desirable example with Pb(1-x/2) Pbx(Zr0.52Ti0.48) (1-x) O3 formula, when x is 0-0.05, Nb compensates the charge generated by the vacancy (vacancy) of Pb (compensate). The dielectric layer 22 which carries out spin coating of the safe PNZT coating solution on the 1st metal layer 20 at the end, and consists of PNZT is obtained.

[0021] It returns to drawing 2 and the 2nd metal layer 24 is formed on a dielectric layer 22. The 2nd metal layer 24 is made to vapor-deposit by approach like sputtering.

[0022] Subsequently, as shown in drawing 3 , pattern NINGU of the 2nd metal layer 24 and the dielectric layer 22 is carried out at the already set-up configuration. subsequently, the photolithography approach -- using it -- the 2nd -- the capacitor structure which carries out pattern NINGU of the 1st metal layer 20 and the buffer layer 18 at the already set-up configuration, and has buffer 18A, lower electrode 20A, capacitor thin film 22A, and up electrode 24A is obtained.

[0023] In order to secure strong adhesive strength between lower electrode 20A and the 1st insulating layer 16, buffer layer 18A is used.

[0024] At the following step, as shown in drawing 4 , plasma CVD is used and the 2nd insulating layer 26 which consists of a silicon oxide (SiO2) on an active substrate 10 and the capacitor structure 23 is formed.

[0025] The 1st and 2nd openings 27 and 28 are formed on the 2nd and 1st insulating layers 26 and 16 by the method located in each part of the diffusion field 6 at the following step. As shown in drawing 5 , the 3rd and 4th openings 30 and 32 are formed on the capacitor structure 23 through the 2nd insulating layer 26 by the method to which each parts of the upper part and the lower electrodes 24A and 20A are exposed.

[0026] Subsequently, as shown in drawing 6 , in order to form the interconnect layer which consists of conductive matter like aluminum (aluminum) over all front faces including the interior of openings 27, 28, 30, and 32 and to form the bit line 34, the metal interconnect 36, and the plate line 38, pattern NINGU of the interconnect layer is carried out, and the semi-conductor memory device 100 is obtained.

[0027] It is obvious for permutations, deformation, and modification various by within the limits which this invention explained above is not limited with the example mentioned above and the attached drawing, and does not exceed the technical thought of this invention to be possible in this contractor that has the information usual by the technical field to which this invention belongs.

[0028]

[Effect of the Invention] As compared with the Prior art, this invention added Nb dopant (dopant) to PZT, and made low the leakage current (leakage current) of about 2 order (order) extent.

[0029] Furthermore, this invention carries out spin coating of the PNZT coating solution with the gestalt of sol gel, and can form capacitor thin film 22A on lower electrode 20A at low temperature.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the sectional view showing the semi-conductor memory device which has the ferroelectric capacitor structure concerning this invention.

[Drawing 2] It is the rough sectional view showing the semi-conductor memory device manufacture approach shown in drawing 1 .

[Drawing 3] It is the rough sectional view showing the semi-conductor memory device manufacture approach shown in drawing 1 .

[Drawing 4] It is the rough sectional view showing the semi-conductor memory device manufacture approach shown in drawing 1 .

[Drawing 5] It is the rough sectional view showing the semi-conductor memory device manufacture approach shown in drawing 1 .

[Drawing 6] It is the rough sectional view showing the semi-conductor memory device manufacture approach shown in drawing 1 .

[Drawing 7] Ferroelectric concerning the example of this invention In order to form a thin film, it is the flow chart which shows the process for preparing a sol gel solution coating solution.

[Description of Notations]

22 Dielectric Layer

22A Capacitor thin film

23 Capacitor Structure

36 Metal Interconnect

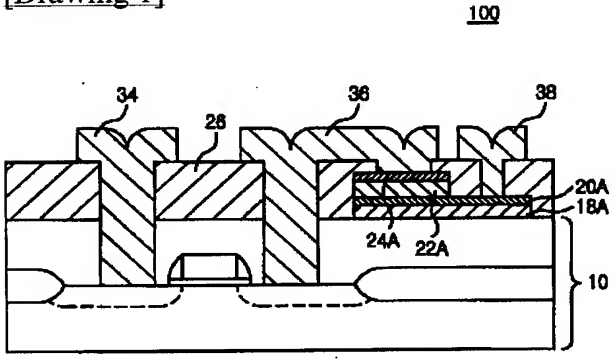
[Translation done.]

* NOTICES *

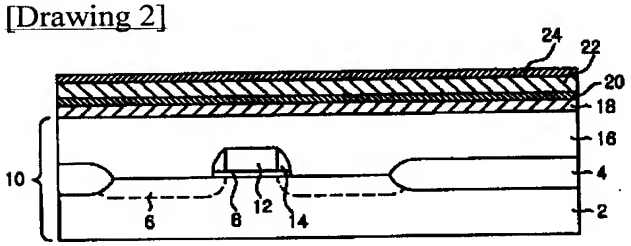
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

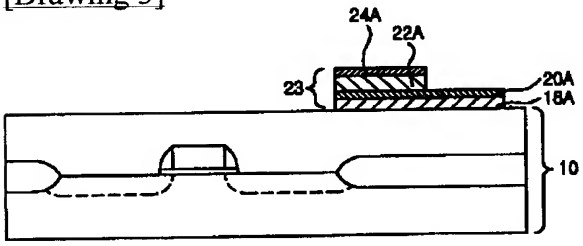
[Drawing 1]



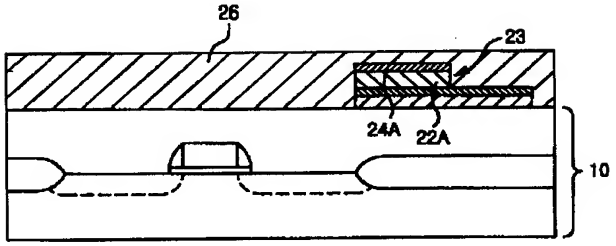
[Drawing 2]



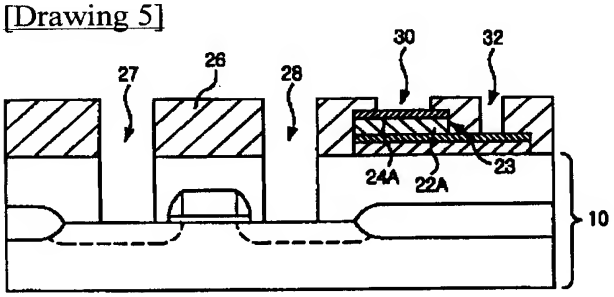
[Drawing 3]



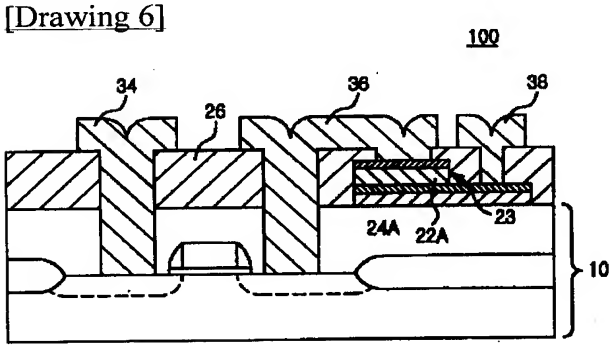
[Drawing 4]



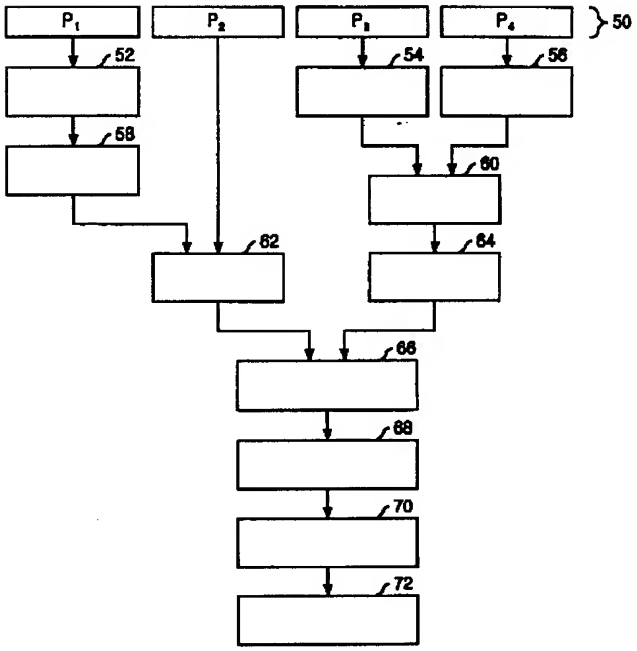
[Drawing 5]



[Drawing 6]



[Drawing 7]



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